



# Micron-scale ion trap in an integrated semiconductor chip



DTO

D. Stick<sup>†</sup>, W.K. Hensinger<sup>†</sup>, M.J. Madsen<sup>†</sup>, S. Olmschenk<sup>†</sup>, D. Hucul<sup>†</sup>, M. Yeo<sup>†</sup>, L. Deslauriers<sup>†</sup>, J. Sterk<sup>†</sup>, K. Schwab<sup>‡</sup>, and C. Monroe<sup>†</sup>

<sup>†</sup> FOCUS Center & Physics Department, University of Michigan

<sup>‡</sup> Laboratory for Physical Sciences



## Semiconductor Fabricated Ion Trap

Future traps will need to be fabricated from a single structure, not manually assembled. One approach is to exploit MEMS techniques in materials such as GaAs/AlGaAs or Si/SiO<sub>2</sub>.

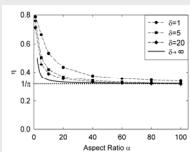
### Design & Simulations

- Linear 2 layer RF trap: RF applied to top cantilevers on one side of gap and bottom cantilevers on the other. All other cantilevers are RF grounded with DC control voltages applied.

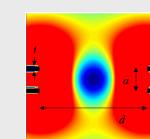
- Semiconductor fabrication restricts design to high aspect ratio geometries (ratio of horizontal cantilever separation to vertical separation)<sup>1</sup>.

- Two layer design easier to fabricate for initial testing.

#### How does aspect ratio affect trap strength?



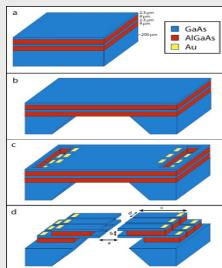
Trap strength efficiency  $\eta$  (scaled to perfect quadrupole trap of same distance between ion and nearest electrode) approaches 1/p for high aspect ratio  $a = da$ . ( $d/a$ ) is ratio between electrode gap  $a$  and electrode thickness  $d$ .



Trap depth transverse to RF node  
1 M.J. Madsen, W.K. Hensinger, D. Stick, J.A. Rabeck, and C. Monroe. Planar ion trap geometry for microfabrication. *Applied Physics B: Laser and Optics* **78**, 639 (2004).

### Fabrication

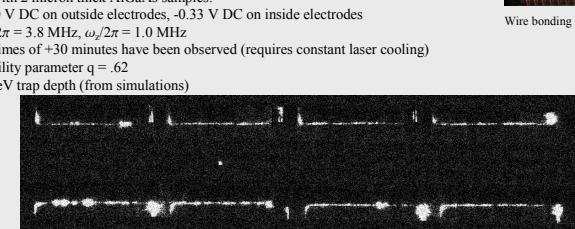
- MBE grown wafer (GaAs substrate) with alternating GaAs and AlGaAs layers. GaAs is heavily doped.
- Backside etch to remove substrate for optical access.
- ICP RIE (Inductively Coupled Plasma Reactive Ion Etcher) etching to substrate (not shown) and second GaAs layer, followed by bond pad evaporation and annealing.
- ICP etch to define cantilevers, and HF etch to remove AlGaAs away from cantilever tips (reduces effect of possible charge buildup).



### Trapping Parameters

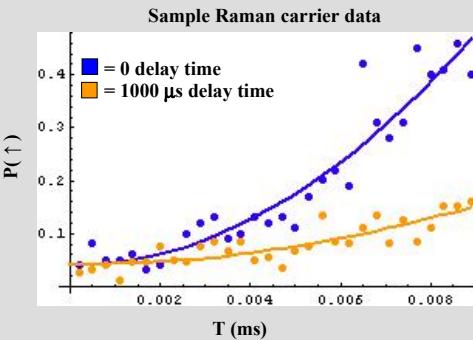
• RF voltage: 8 V applied at 15.9 MHz drive frequency<sup>2</sup>

- This is close to the maximum voltage we can apply to this trap. While we have been able to apply up to 70 V DC between vertical layers, test traps have only been able to withstand 10-15 V RF. We speculate that power dissipation due to the finite capacitance between layers is to blame. We observe that the maximum voltage that can be applied is non-linear with the thickness of the insulator, as seen in comparisons with 2 micron thick AlGaAs samples.

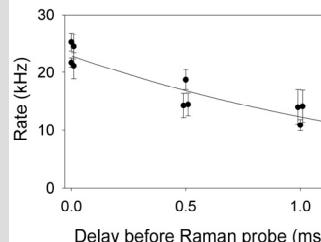


<sup>2</sup> D. Stick, W.K. Hensinger, S. Olmschenk, M.J. Madsen, K. Schwab, and C. Monroe. Ion Trap in a Semiconductor Chip. *Nature Physics*, **2**, 36-39 (2006).

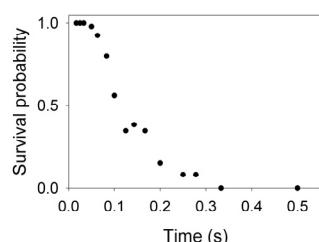
## Ground State Motional Heating in the Microtrap



### Suppression of Raman transition rate



### Boil off rate of ion



<sup>3</sup> L. Deslaurier, et al. *eprint quant-ph/0602003*

<sup>4</sup> Private communication, G. Milburn.

This heating rate is larger than what we would expect from measurements of heating rate scaling laws with electrode-ion distance<sup>3</sup>, by about a factor of 20. Possible sources of this include the fact that the substrate is cracked, and so the electrodes aren't perfectly aligned, neither vertically nor horizontally. This could lead to a bias field that we cannot compensate for, or could be the result of an ungrounded substrate which gets charged up. Another theory is that the piezo-electric effect in GaAs contributes to the heating<sup>4</sup>. While this would produce a resonance at the same frequency as the moving cantilever, it would have a much lower Q, and could therefore overlap with the ion's motion. Experiments are planned in which we use a laser interferometer to measure the spectrum of motion of the cantilevers.

## Future Silicon Trap Fabrication

One alternative fabrication technique to the GaAs traps is to use a similar layer structure of silicon and silicon oxide. The processing would be relatively similar, with KOH being the selective etch for silicon, HF (or buffered oxide etch) being used for the oxide etch, and a reactive ion etcher for the dry etching. The advantages are that the silicon oxide is a much better insulator than AlGaAs. Although doped silicon will be more resistive than doped GaAs, the heat dissipation will be offset by the higher dielectric constant of silicon oxide.

